Stratix GX FPGA Family

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Introduction

The Stratix® GX family of devices is Altera's second FPGA family to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES capability at data rates of up to 3.1875 gigabits per second (Gbps). These transceivers are grouped by four-channel transceiver blocks, and are designed for low power consumption and small die size. The Stratix GX FPGA technology is built upon the Stratix architecture, and offers a 1.5-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

- Transceiver block features are as follows:
  - High-speed serial transceiver channels with CDR provides 500-megabits per second (Mbps) to 3.1875-Gbps full-duplex operation
  - Devices are available with 4, 8, 16, or 20 high-speed serial transceiver channels providing up to 127.5 Gbps of full-duplex serial bandwidth
  - Support for transceiver-based protocols, including 10 Gigabit Ethernet attachment unit interface (XAUI), Gigabit Ethernet (GigE), and SONET/SDH
  - Compatible with PCI Express, SMPTE 292M, Fibre Channel, and Serial RapidIO I/O standards
  - Programmable differential output voltage (V_{OD}), pre-emphasis, and equalization settings for improved signal integrity
  - Individual transmitter and receiver channel power-down capability implemented automatically by the Quartus® II software for reduced power consumption during non-operation
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, and 20-bit wide data paths
  - 1.5-V pseudo current mode logic (PCML) for 500 Mbps to 3.1875 Gbps
  - Support for LVDS, LVPECL, and 3.3-V PCML on reference clocks and receiver input pins (AC-coupled)
  - Built-in self test (BIST)
  - Hot insertion/removal protection circuitry

- Pattern detector and word aligner supports programmable patterns
- 8B/10B encoder/decoder performs 8- to 10-bit encoding and 10- to 8-bit decoding
- Rate matcher compliant with IEEE 802.3-2002 for GigE mode and with IEEE 802-3ae for XAUI mode
- Channel bonding compliant with IEEE 802.3ae (for XAUI mode only)
- Device can bypass some transceiver block features if necessary

- FPGA features are as follows:
  - 10,570 to 41,250 logic elements (LEs); see Table 1
  - Up to 3,423,744 RAM bits (427,968 bytes) available without reducing logic resources
  - TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in-out (FIFO) buffers
  - Up to 16 global clock networks with up to 22 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (faster than 300 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to eight general usage phase-locked loops (four enhanced PLLs and four fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switchover, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 45 channels for 1-Gbps performance
  - Support for source-synchronous bus standards, including 10-Gigabit Ethernet XSBI, Parallel RapidIO, UTOPIA IV, Network Packet Streaming Interface (NPSI), HyperTransport™ technology, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
  - Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  - Support for remote configuration updates
  - Dynamic phase alignment on LVDS receiver channels

Table 1. Stratix GX Device Features

Feature	EP1SGX10C EP1SGX10D	EP1SGX25C EP1SGX25D EP1SGX25F	EP1SGX40D EP1SGX40G
LEs	10,570	25,660	41,250
Transceiver channels	4, 8	4, 8, 16	8, 20
Source-synchronous channels	22	39	45
M512 RAM blocks (32 × 18 bits)	94	224	384
M4K RAM blocks (128 × 36 bits)	60	138	183
M-RAM blocks (4K ×144 bits)	1	2	4
Total RAM bits	920,448	1,944,576	3,423,744
Digital signal processing (DSP) blocks	6	10	14
Embedded multipliers *(1)*	48	80	112
PLLs	4	4	8

Note to Table 1:

(1) This parameter lists the total number of 9- × 9-bit multipliers for each device. For the total number of 18- × 18-bit multipliers per device, divide the total number of 9- × 9-bit multipliers by 2. For the total number of 36- × 36-bit multipliers per device, decide the total number of 9- × 9-bit multipliers by 8.

Stratix GX devices are available in space-saving FineLine BGA® packages (refer to Tables 2 and 3), and in multiple speed grades (refer to Table 4). Stratix GX devices support vertical migration within the same package (that is, the designer can migrate between the EP1SGX10C and EP1SGX25C devices in the 672-pin FineLine BGA package). See the Stratix GX device pin tables for more information. Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type, to identify which I/O pins it is possible to migrate. The Quartus II software can automatically cross reference and place all pins for migration when given a device migration list.

Table 2. Stratix GX Package Options & I/O Pin Counts (Part 1 of 2) *Note (1)*

Device	672-Pin FineLine BGA	1,020-Pin FineLine BGA
EP1SGX10C	362	
EP1SGX10D	362	
EP1SGX25C	455	

Table 2. Stratix GX Package Options & I/O Pin Counts (Part 2 of 2) *Note (1)*

Device	672-Pin FineLine BGA	1,020-Pin FineLine BGA
EP1SGX25D	455	607
EP1SGX25F		607
EP1SGX40D		624
EP1SGX40G		624

Note to Table 2:
(1) The number of I/O pins listed for each package includes dedicated clock pins and dedicated fast I/O pins. However, these numbers do not include high-speed or clock reference pins for high-speed I/O standards.

Table 3. Stratix GX FineLine BGA Package Sizes

Dimension	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00
Area (mm^2)	729	1,089
Length × width (mm × mm)	27 × 27	33 × 33

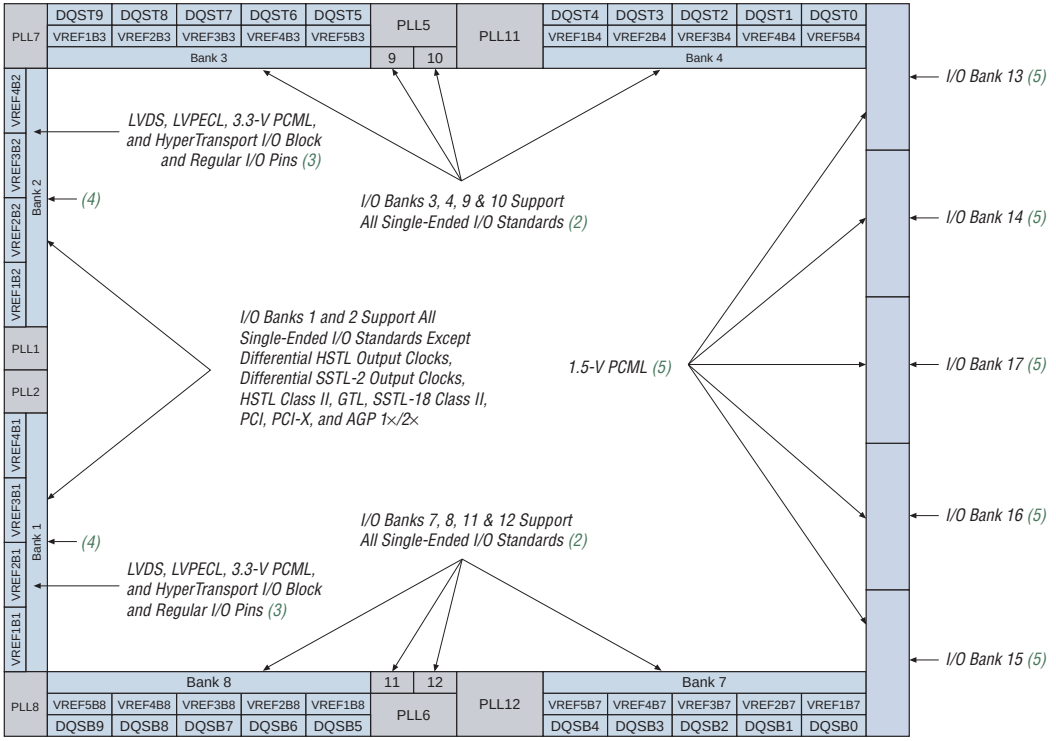
Table 4. Stratix GX Device Speed Grades

Device	672-Pin FineLine BGA	1,020-pin FineLine BGA
EP1SGX10	-5, -6, -7	
EP1SGX25	-5, -6, -7	-5, -6, -7
EP1SGX40		-5, -6, -7

High-Speed I/O Interface Functional Description

The Stratix GX device family supports high-speed serial transceiver blocks with CDR circuitry as well as source-synchronous interfaces. The channels on the right side of the device use an embedded circuit dedicated for receiving and transmitting high-speed serial data streams to and from the system board. These channels are clustered in a four-channel serial transceiver building block and deliver high-speed bidirectional point-to-point data transmissions to provide up to 3.1875 Gbps of full-duplex data transmission per channel. The channels on the left side of the device support source-synchronous data transfers at up to 1 Gbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards. Figure 1 shows the Stratix GX I/O blocks. The differential source-synchronous serial interface is described in "Principles of SERDES Operation" on page 47 and the high-speed serial interface is described in "Transceiver Blocks" on page 8.

Figure 1. Stratix GX I/O Blocks *Note (1)*



Notes to Figure 1:

(1) Figure 1 is a top view of the Stratix GX silicon die.

(2) Banks 9 through 12 are enhanced PLL external clock output banks.

(3) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X, and AGP 1×/2×.

(4) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook*, Volume 2.

(5) These I/O banks in Stratix GX devices also support the LVDS, LVPECL, and 3.3-V PCML I/O standards on reference clocks and receiver input pins (AC coupled).

FPGA Functional Description

Stratix GX devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

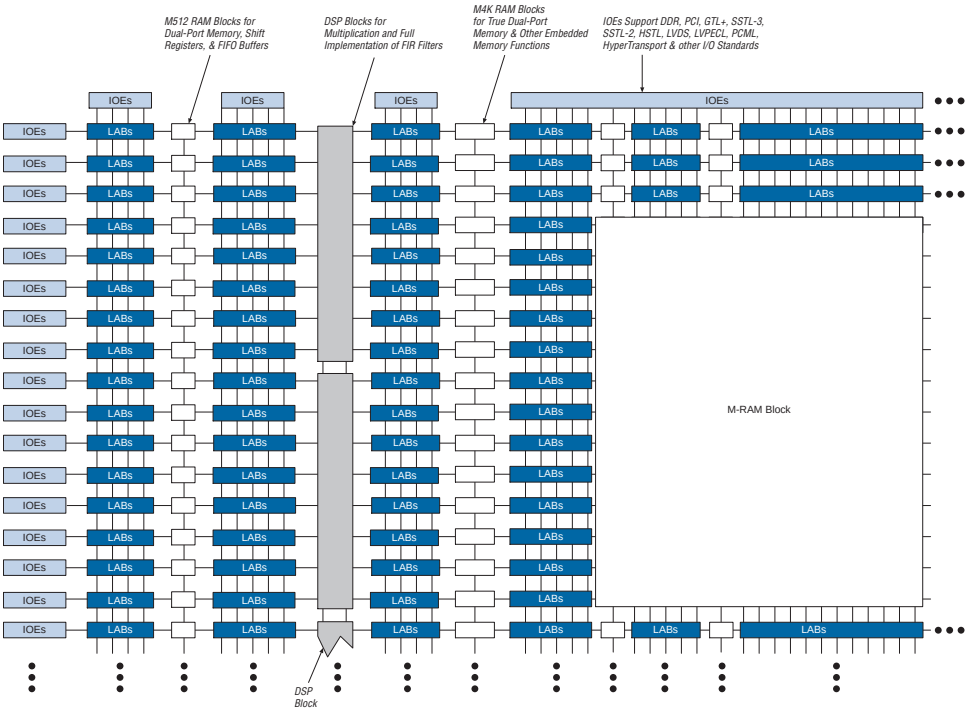
Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix GX device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM, FCRAM, ZBT, and QDR SRAM devices.

High-speed serial interface channels support transfers at up to 840 Mbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards.

Figure 2 shows an overview of the Stratix GX device.

Figure 2. Stratix GX Block Diagram



The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 5 lists the resources available in Stratix GX devices.

Table 5. Stratix GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP1SGX10	4 / 94	2 / 60	1	2 / 6	40	30
EP1SGX25	6 / 224	3 / 138	2	2 / 10	62	46
EP1SGX40	8 / 384	3 / 183	4	2 / 14	77	61

Transceiver Blocks

Stratix GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.1875-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 3.1875 Gbps of data transition per channel.

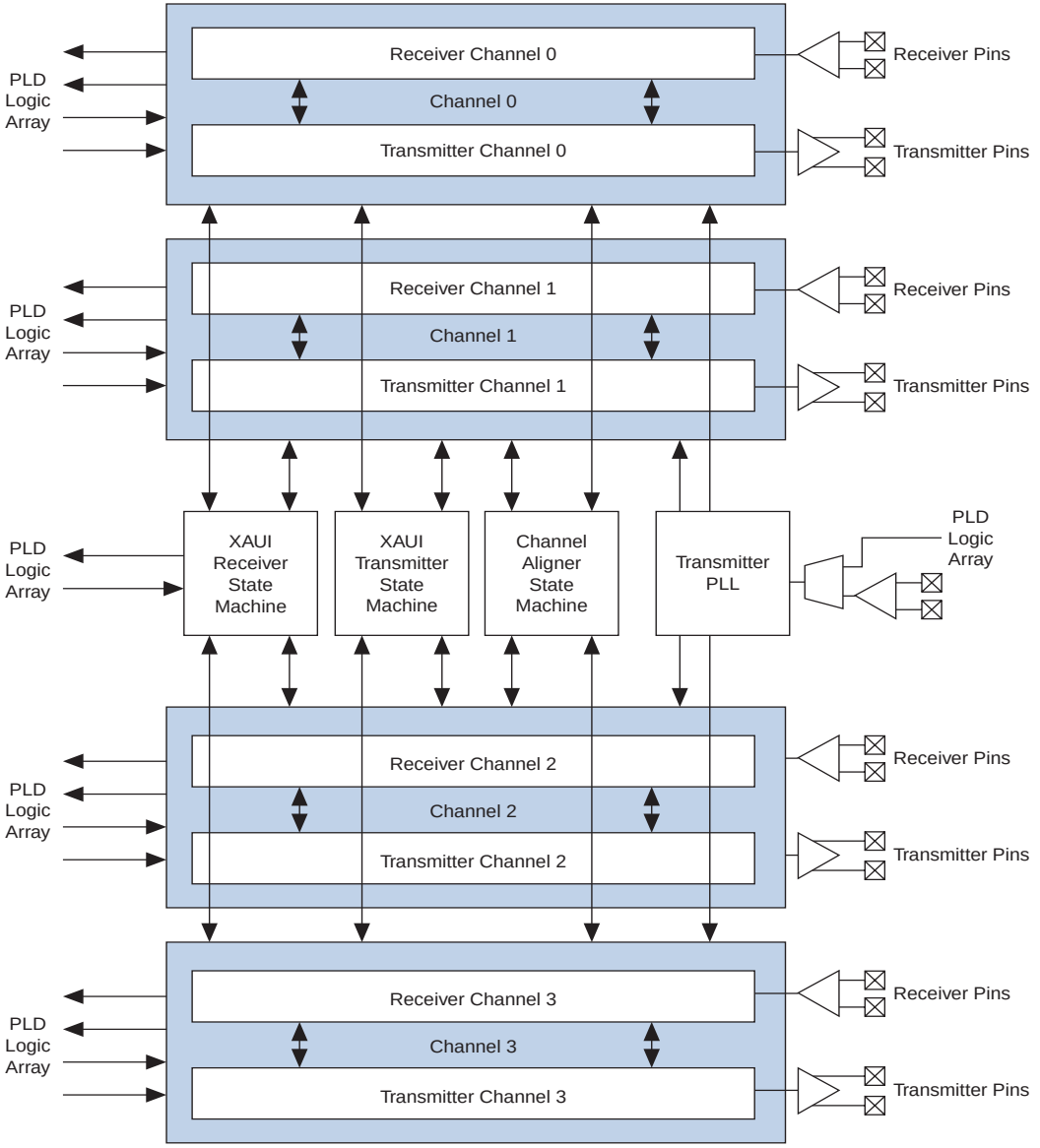
There are up to 20 transceiver channels available on a single Stratix GX device. Table 6 shows the number of transceiver channels available on each Stratix GX device.

Table 6. Stratix GX Transceiver Channels

Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

Figure 3 shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching for XAUI and GigE applications, in addition to channel bonding for XAUI applications.

Figure 3. Stratix GX Transceiver Block



Each Stratix GX transceiver channel consists of a transmitter and receiver. The transmitter contains the following:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

The receiver contains the following:

- Input buffer
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

Designers can set all the Stratix GX transceiver functions through the Quartus II software. Designers can set programmable pre-emphasis, programmable equalizer, and programmable V_{OD} dynamically as well. Each Stratix GX transceiver channel is also capable of BIST generation and verification in addition to various loopback modes. Figure 4 shows the block diagram for the Stratix GX transceiver channel.

Stratix GX transceivers provide physical coding sublayer (PCS) and physical media attachment (PMA) implementation for protocols such as 10-gigabit XAUI and GigE. The PCS portion of the transceiver consists of the logic array interface, 8B/10B encoder/decoder, pattern detector, word aligner, rate matcher, channel aligner, and the BIST and pseudo-random binary sequence pattern generator/verifier. The PMA portion of the transceiver consists of the serializer/deserializer, the CRU, and the I/O buffers.